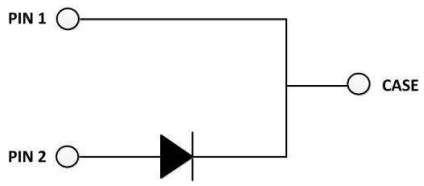
Powerex, Inc., 173 Pavilion Lane, Youngwood, Pennsylvania 15697 (724) 925-7272
www.pwrx.com

3rd Generation 650V/50A SiC Schottky Barrier Diode

PDS050J065H3

Circuit diagram



Package Type: TO-247-2L

HF

RoHS

Description

The PDS050J065H3 SiC Schottky Barrier Diode (SBD) has been developed using Powerex's advanced 3rd generation SiC SBD technology with the highest performance and reliability. It registers higher efficiency, higher operation temperature and lower loss and can be operated at higher frequency than Si-based solutions. As to the Schottky structure, it shows no recovery at turn-off and allows a low leakage current with reverse voltage up to 650V. It can contribute to system miniaturization and achieve lightweight system design. Using RoHS compliant components, it is qualified for use in industrial application.

Features

- Revolutionary semiconductor material - Silicon Carbide (SiC)
- No reverse recovery
- High-speed switching performance
- Temperature-independent switching behavior
- System cost / size savings due to reduced cooling requirements
- Junction temperature range from -55°C to 175°C
- RoHS compliant

Applications

- Industrial power supplies: Industrial UPS
- Battery chargers
- Solar inverters
- Switch mode power supplies

Product Specifications

Device	V_{RRM}	I_F (135°C)	V_F (25°C)	Q_C	Marking
PDS050J065H3	650V	57A	1.35V	138nC	PDS050J065H3

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Contents

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Maximum Ratings (T_c = 25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit	Test conditions
Repetitive peak reverse voltage	V_{RRM}	650	V	T_C = 25℃
Surge peak reverse voltage	V_{RSM}	650		T_C = 25℃
DC reverse voltage	V_{DC}	650		T_C = 25℃
Continuous forward current	I_F	114	A	T_C = 25℃
		57		T_C = 135℃
		50		T_C = 143℃
Surge non-repetitive forward current	I_{FSM}	337	A	T_C = 25℃, t_p = 10ms, half sine pulse
Surge repetitive forward current	I_{FRM}	207	A	T_C = 25℃, t_p = 10ms, half sine wave D = 0.1
Power dissipation	P_{tot}	348	W	T_C = 25℃
i^2t value	$\int i^2dt$	567	A^2s	T_C = 25℃, t_p = 10ms
Operating junction temperature	T_j	-55~175	℃	
Storage temperature	T_{stg}	-55~175	℃	
Mounting torque	M	1	Nm	M3 screw

Thermal Resistance

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Thermal resistance from junction to case	$R_{th(j-c)}$	/	0.43	/	℃/W	

Static Electrical Characteristics (T_j = 25°C, unless otherwise specified)

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
DC blocking voltage	V_{DC}	650	/	/	V	I_R = 100 μA
Forward voltage	V_F	/	1.35	1.50	V	I_F = 50A, T_j = 25℃
		/	1.60	1.90		I_F = 50A, T_j = 175℃
Reverse current	I_R	/	5	120	μA	V_R = 650V, T_j = 25℃
		/	20	300		V_R = 650V, T_j = 175℃

Dynamic Electrical Characteristics (T_j = 25°C, unless otherwise specified)

Parameter	Symbol	Values			Unit	Test conditions
		Min.	Typ.	Max.		
Total capacitance	C	/	2970	/	pF	V_R = 0V, f = 1MHz
		/	255	/		V_R = 200V, f = 1MHz
		/	222	/		V_R = 400V, f = 1MHz
Total capacitive charge	Q_C	/	138	/	nC	V_R = 400V
Capacitance stored energy	E_C	/	20	/	μJ	V_R = 400V

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Electrical Characteristic Diagrams

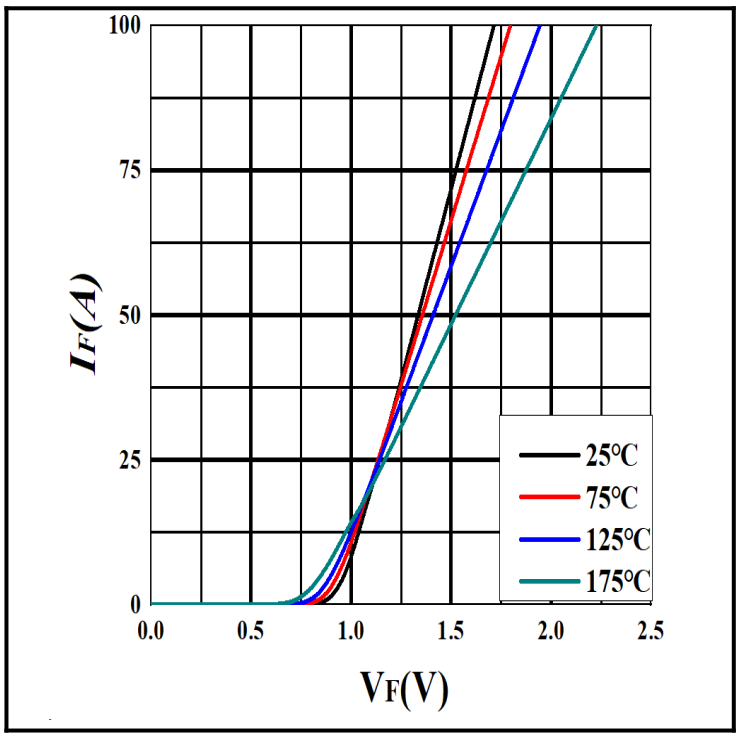

Figure 1. Forward characteristics

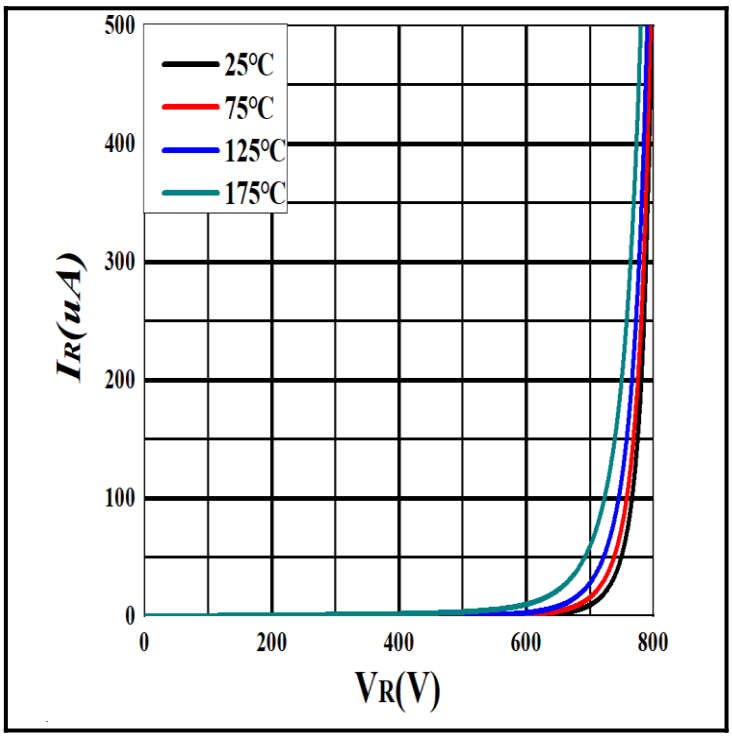

Figure 2. Reverse characteristics

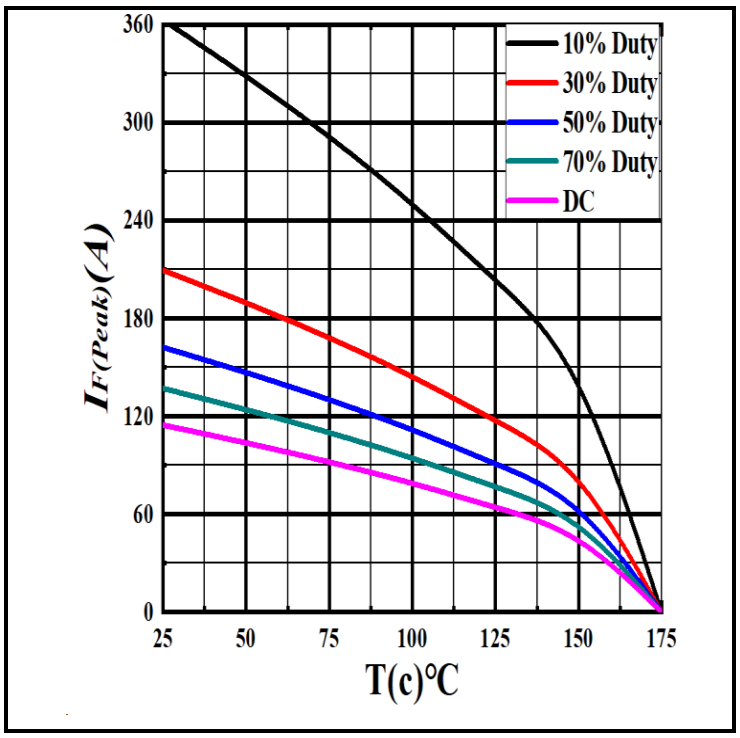

Figure 3. Current derating

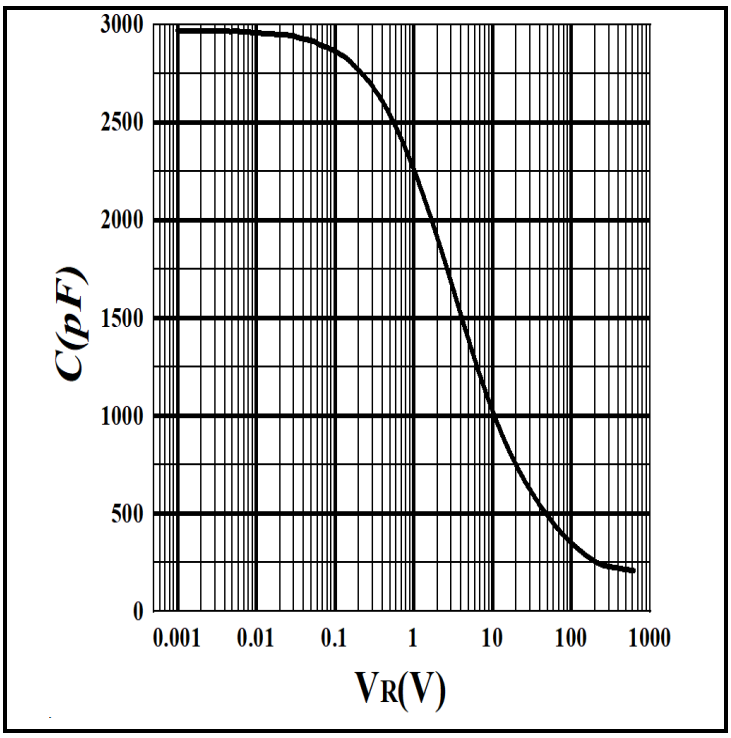

Figure 4. Capacitance vs. reverse voltage

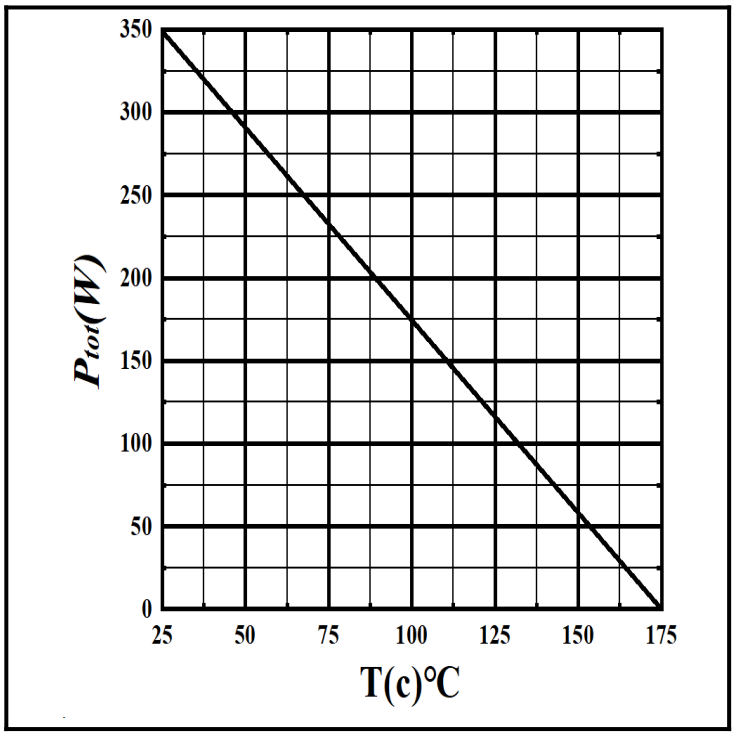

Figure 5. Power derating

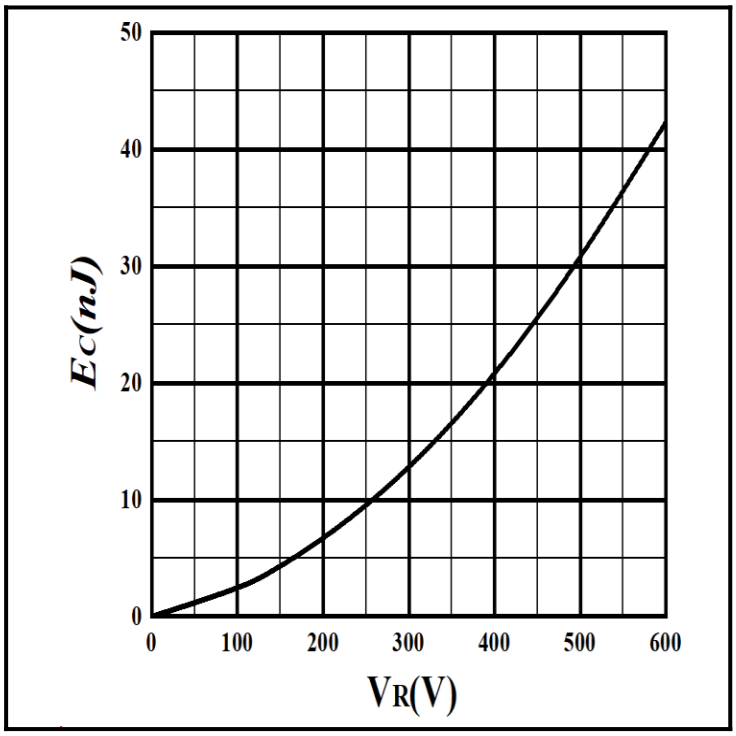

Figure 6. Capacitance stored energy

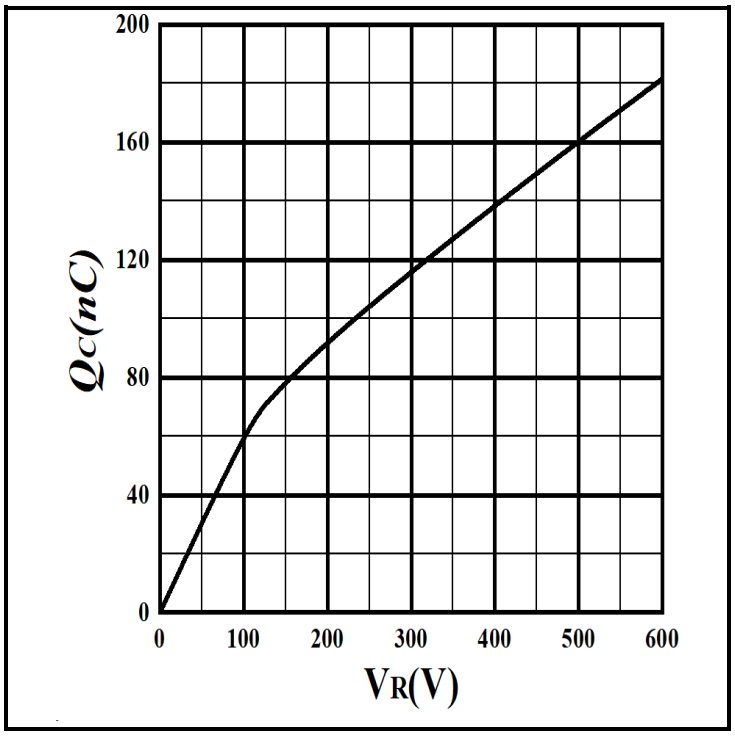

Figure 7. Total capacitance charge vs. reverse voltage

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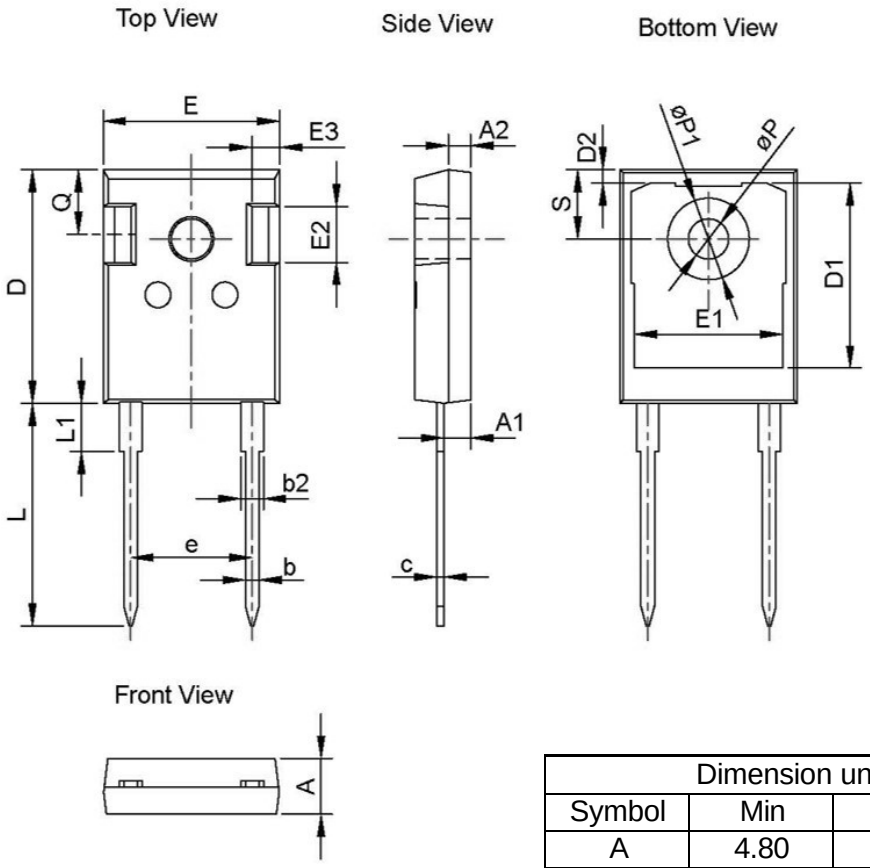
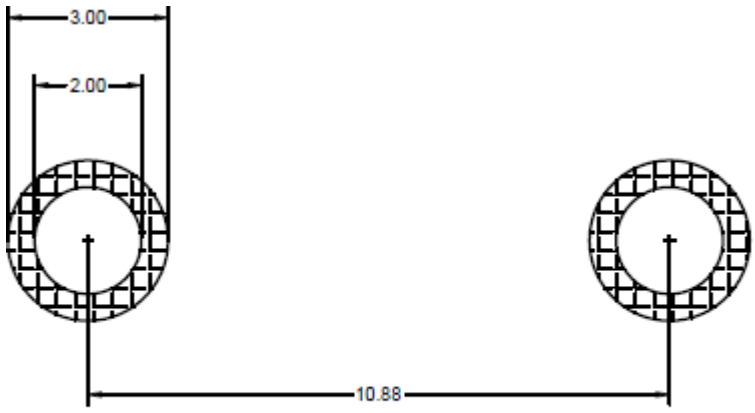
Package Information



Dimension unit: [mm]			
Symbol	Min	Nom	Max
A	4.80	5.00	5.20
A1	2.21	2.41	2.61
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b2	1.91	2.01	2.21
c	0.51	0.60	0.75
D	20.70	21.00	21.30
D1	16.25	16.55	16.85
D2	1.00	1.20	1.35
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.80	5.00	5.20
E3	2.30	2.50	2.70
e	10.88 BSC		
L	19.62	19.92	20.22
L1	-	-	4.30
øP	3.40	3.60	3.80
øP1	-	-	7.30
Q	5.40	5.80	6.20
S	6.20 BSC		

Recommended Solder Pad Layout



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Note: All dimensions are in mm